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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
Brown 9-2

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Application Number	Filed
10/799,239	2004-03-12

First Named Inventor: D.A. Brown et al.

Art Unit	Examiner
2416	Ben H. Liu

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☑ attorney or agent of record. Registration number 37,922.
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

Signature

Joseph B. Ryan
Typed or printed name

516-759-7517
Telephone number

October 28, 2009
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): D.A. Brown et al.
Case: 9-2
Serial No.: 10/799,239
Filing Date: March 12, 2004
Group: 2416
Examiner: Ben H. Liu

Title: Processor Having Split Transmit and Receive Media Access Controller with Reduced Complexity Interface

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REMARKS FOR PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicants request review of the final rejection, dated July 28, 2009, in the above-identified application. No amendments are being filed with this request. A Notice of Appeal is submitted concurrently herewith. Applicants incorporate by reference herein all responses previously filed in the above-identified application.

The present application was filed on March 12, 2004 with claims 1-22. Claims 1-22 are currently pending in the application. Claims 1 and 17-19 are the independent claims.

Claims 1, 3, 5, 7-17, 19, 21 and 22 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 7,197,045 (hereinafter "Amit") in view of U.S. Patent No. 6,963,535 (hereinafter "Stark").

Claims 2, 4, 6, 18 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Amit and Stark in view of other references.

Independent claim 1 recites that the first and second split transmit and receive media access controllers have respective distinct addresses encoded by particular values of information bits sent over the interface, and further that the processor decodes said information bits so as to distinguish a first signal sent between the transmit and receive units of the first split transmit and receive media access controller from a second signal sent between the transmit and receive units of the second split transmit and receive media access controller.

For example, the diagram of FIG. 6 illustrates the address decoding for distinguishing carrier sense signals sent between transmit and receive units of 32 different split transmit and receive MACs. See page 9, line 26, to page 10, line 7, and page 12, line 21, to page 13, line 2. As another

example, FIG. 8 illustrates the address decoding for distinguishing deference reset signals sent between transmit and receive units of 16 different split transmit and receive MACs. The recited interface is advantageous in that it allows numerous split transmit and receive MACs to communicate over a common interface in a particularly efficient and flexible manner. See the specification at, for example, page 17, lines 5-10.

In arguing that the combination of Amit and Stark meets this limitation of claim 1, the Examiner relies on column 5, lines 1-14, of Amit, which the Examiner characterizes as teaching a "CPU 230 that utilizes information bits to distinguish signals belonging a [sic] first and second transmitter and a second information bit to distinguish signals belonging a [sic[first and second receiver." Applicants respectfully note that the relied-upon portion of Amit in fact states, with added emphasis:

> The CPU 230 is adapted to specify to each data packet which transmitter 234 to be sent to, for example, the CPU 230 may send a "0" to indicate the packet should be sent to transmitter 1, and the CPU 230 may send a "1" to indicate that the packet should be sent to transmitter 2 (not shown; however, dual transmitter 234 comprises transmitter 1 and 2.) Similarly, a bit may be used by the CPU 230 to indicate if a packet came from receiver 1 or from receiver 2 (not shown; however, dual receiver 236 comprises receiver 1 and 2.)

It is clear that the CPU is assigning these bits to indicate to which transmitter or receiver the packet belongs, and hence the CPU must already know to which transmitter or receiver the packet belongs. In any case, there is no teaching or suggestion that the CPU - or any processor - performs any decoding of these bits, much less that such decoding is performed to distinguish between signals in the manner specified in claim 1. Stark fails to remedy the fundamental deficiency of Amit with regard to this limitation of claim 1, and thus claim 1 is patentable over Amit and Stark.

Moreover, the Examiner acknowledges that Amit fails to meet the recited interface that is configured to multiplex signals directed between the transmit unit and the receive unit of a first split transmit and receive media access controller (MAC) with signals directed between a transmit unit and a receive unit of at least a second split transmit and receive MAC. However, the Examiner argues that Stark meets these recitations, relying on the abstract, column 3, lines 19-20, and FIG. 3 of Stark. Applicants respectfully disagree.

It is important to point out that a particular type of multiplexing is recited in the above-noted portion of claim 1, rather than multiplexing in general. The interface set forth in the claim is

expressly described as being configured to multiplex signals that are directed between the transmit unit and the receive unit of a first split transmit and receive MAC with signals that are directed between a transmit unit and a receive unit of a second split transmit and receive MAC.

The arrangement shown in FIG. 3 of Stark and relied upon by the Examiner clearly fails to provide the particular type of multiplexing recited in claim 1. FIG. 3 shows an arrangement which includes multiplexers 22 and 24, a buffer 10, and multiple MACs 12A, 12B and 12C. The multiplexers 22 and 24 multiplex signals directed between one of the MACs 12 and the buffer 10 with signals directed between another one of the MACs 12 and the buffer 10. For example, signals directed between the MAC 12A and the buffer 10 are multiplexed with signals that are directed between the MAC 12B and the buffer 10. This is an entirely different type of multiplexing than that recited in claim 1. The MACs 12 in FIG. 3 of Stark are not split transmit and receive MACs, nor does Stark disclose any interface which multiplexes signals that are directed between a transmit unit and a receive unit of a first split MAC with signals that are directed between a transmit unit and a receive unit of a second split MAC. To the contrary, the MACs 12 of Stark are apparently entirely separate and self-contained, each comprising both transmit and receive functionality, such that any signals directed between transmit and receive units of a given such MAC 12 do not pass through multiplexers 22 or 24 at all.

It is therefore respectfully submitted that the teachings of Stark fail to supplement the deficiencies of Amit as applied to the interface multiplexing arrangement of claim 1. The collective teachings of Amit and Stark simply fail to meet the recitations of the claim. They also fail to provide the considerable advantages associated with illustrative embodiments of the claimed invention. See the specification at, for example, page 17, lines 5-10.

Moreover, it is believed that one skilled in the art would not be motivated to combine or modify Amit and Stark to meet the claimed invention. The Examiner apparently argues that it would be obvious to combine Amit and Stark by coupling the MAC bus as taught by Stark between the CPU 330 and the switch 352 shown in FIG. 6 of Amit. See the Office Action at page 4, lines 3-11. However, this proposed modification of Amit would be inappropriate and unworkable. As noted above, the MAC bus comprising multiplexers 22 and 24 in FIG. 3 of Stark is used to multiplex signals directed between one MAC and a buffer with signals directed between another entirely separate MAC and that same buffer. As Applicants noted in their previous response, with reference to FIG. 6 of Amit, it is indicated in column 5, lines 30-33, that Base MAC 338 is part of a single split

MAC and corresponds to transmitter MAC 138 of FIG. 4, and it is indicated in column 5, lines 40-43, that Base MAC 340 is part of the same split MAC and corresponds to receiver MAC 140 of FIG. 4. The Base MACs 338 and 340 may therefore be viewed as transmit and receive portions of a single split MAC. Thus, there would be no motivation to implement the MAC bus of Stark, which multiplexes signals directed between one MAC and a buffer with signals directed between another MAC and that buffer, in the single split MAC arrangement in FIG. 6 of Amit. Stark in fact teaches away from the claimed arrangement by teaching that each of the MACs 12 is apparently entirely self-contained, such that any signals directed between transmit and receive portions of a given such MAC 12 do not even pass through the MAC bus comprising multiplexers 22 and 24. See Stark at column 2, line 65, to column 3, line 15.

For the above reasons, it is respectfully submitted that the collective teachings of Amit and Stark fail to meet the limitations of independent claim 1.

Independent claims 17-19 are believed patentable for reasons similar to those outlined above with regard to claim 1.

Dependent claims 3, 5, 7-16, 21 and 22 are believed patentable for at least the reasons given above for their respective independent claims.

With regard to the §103(a) rejections of claims 2, 4, 6, 18 and 20, the additional cited references fail to supplement the fundamental deficiencies of Amit and Stark as applied to the independent claims.

The dependent claims are also believed to define separately patentable subject matter relative to the cited references.

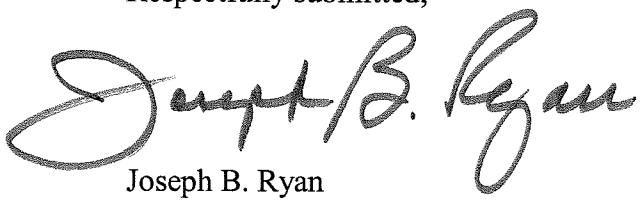
For example, dependent claim 4 specifies that the interface is controllably operable in one of at least two modes including an internal mode of operation, in which the interface is configured to deliver signals between one or more transmit units and one or more receive units where the transmit units and the receive units are implemented on the same integrated circuit, and an external mode of operation, in which the interface is configured to deliver signals between one or more transmit units and one or more receive units where the transmit units and the receive units are implemented on different integrated circuits. The Examiner apparently acknowledges that the collective teachings of Amit and Stark fail to meet these limitations, but argues that they are shown in column 8, lines 10-19, and FIG. 3 of U.S. Patent No. 6,256,306 (hereinafter "Bellenger"). However, the relied-upon portions of Bellenger clearly fail to teach or suggest the recited interface operable in internal and

external modes of operation as recited in claim 4. In fact, there is no mention whatsoever in Bellenger of an interface operable in such modes. The collective teachings of Amit, Stark and Bellenger therefore fail to meet the limitations of claim 4.

As another example, dependent claim 5 specifies that the interface comprises a receive interface block coupled to a generate interface block via an interface bus, the generate interface block receiving signals from a plurality of media access controller receive units and multiplexing the signals onto the interface bus for delivery to the receive interface block, the receive interface block demultiplexing the signals from the interface bus for delivery to appropriates ones of a plurality of media access controller transmit units. The Examiner apparently acknowledges that Amit fails to meet these limitations, but argues that they are shown in the MAC bus of FIG. 3 in Stark. See the Office Action in the last paragraph beginning on page 4. However, as indicated previously herein, the relied-upon portions of Stark relate to multiplexing signals directed between one MAC 12 and a buffer 10 with signals directed between another entirely separate MAC 12 and the buffer 10. Accordingly, the MAC bus of Stark fails to teach or suggest the recited generate interface block and receive interface block performing respective multiplexing and demultiplexing operations. Illustrative embodiments of such elements are shown as elements 304 and 306 in FIG. 3 of the present application. There are simply no analogous elements in the MAC bus of Stark, which as noted above provides an entirely different type of multiplexing than that at issue in the present application. The collective teachings of Amit and Stark therefore fail to meet the limitations of claim 5.

In view of the above, Applicants believe that claims 1-22 are in condition for allowance, and respectfully requests withdrawal of the §103(a) rejections.

Respectfully submitted,



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